REMARKS

Claims 1, 3, 11-15 and 19-24 are pending for further examination.

Claims 4-10 and 17-18 were withdrawn from further consideration as the result of a restriction requirement.

Claims 19-21 have been amended to address the objection to those claims. In view of the amendments to those claims, applicant respectfully requests withdrawal of the objections.

The references to a "thick" gate insulating film and a "high voltage" MOS transistor have been removed from the pending claims. Therefore, applicant respectfully requests withdrawal of the rejections of the claims under 35 U.S.C. § 112, par. 2.

In view of claim 16 being canceled, the rejection of that claim 35 U.S.C. § 112, par. 1 is moot.

Claims 1, 3, 11-15 and 19-21 were rejected over the combination of the Komori et al. patent and the Hsieh et al. patent. As discussed below, applicant respectfully requests reconsideration.

Independent claims 1, 11 and 13 recite "simultaneously and selectively forming the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor in a single thermal oxidation step." An example of that feature is illustrated in FIGS. 3 and 4 of the pending application in which the oxide 12 and the gate insulating film 13 are formed at the same time.

The Komori et al. patent discloses a technique for manufacturing an integrated circuit with a non-volatile memory element Qm and MISFETs Qn, Qp. As part of that process, an oxide film 8 is formed over the entire surface (*see* FIG. 8). Contrary to Office action, the oxide film 8 is not "simultaneously" formed over the areas for the non-volatile memory element and the MISFETS. Instead, the Komori et al. patent indicates that, although the oxide film 8 over the MISFETs may be obtained using substantially the same process steps as the oxide film 8 over the

memory element, the different oxide films 8 are provided during different steps at different times:

> Next, in the region wherein the flash type non-volatile memory element Qm is formed there is formed a second gate insulating film 8 on the surface of the electroconductive film 7A. By a manufacturing step substantially the same step, as this step, a second gate insulating film 8 is formed on the major surface of each of the p-type well regions 3 corresponding to the n-channel MISFET Qn forming regions of the semiconductor substrate and on the major surface of each of then-type well regions 2 corresponding to the p-channel MISFET Qp forming regions of the semiconductor substrate.

(Col. 8, lines 23-33)

Furthermore, as acknowledged by the Office action, the Komori et al. patent does not disclose "selectively" forming the oxide film on the floating gate and the gate insulating film. Instead, the gate insulating film(s) 8 is formed over the entire surface (*see* FIG. 4). The Office action, however, relies on the Hsieh et al. patent as disclosing selectively forming an oxide film (*e.g.*, polyoxide 45 in FIG. 2d). The Office action also relies on that patent, in connection with independent claims 11 and 13, for its disclosure of forming an oxidation-resistant film over the entire surface and selectively removing the oxidation-resistant film (*see, e.g.*, FIGS. 2b and 2c in which reference numeral 50 identifies a nitride layer).

Applicant acknowledges the foregoing disclosure of the Hsieh et al. patent, but submits that there would have been no motivation to combine that disclosure with the disclosure of the Komori et al. patent so as to obtain the subject matter of the pending claims.

In particular, as already noted above, the gate insulating film(s) 8 in the Komori et al. patent is formed over the entire surface. Although the gate insulating film is removed from much of the area of he memory element other than the information storing gate 7 (*see* FIG. 5), that film remains over the *entire* area of the MISFETs Qn, Qp through many subsequent processing steps (*see* FIGS 5, 6, 7, 8, 9, and 10). The film 8 in the area of the MISFETs is only

partially removed after an interlayer insulating film 19 is deposited on the whole substrate surface and through-holes 20 are finally formed so that wiring lines 21 can be provided (col. 10, line 66 – col. 11, line 5; FIG. 1). Thus, it is clear that, according to the Komori et al. patent, it is desirable to retain the insulating film 8 over the *entire* surface of the area of the MISFETs for many processing steps, including those of FIGS. 5-10. To selectively form the insulating film 8 initially only in the regions as shown in FIG. 1 would be contrary to the techniques of the Komori et al. patent.

In addition, the Hsieh et al. patent relates to the fabrication of a memory cell, but not to the fabrication of MISFETs or MOS transistors. Therefore, even if there were some motivation to use the disclosure of the Hsieh et al. patent (regarding the formation and selective removal of an oxidation-resistant film and the selective formation of an oxide) in combination with the Komori et al. patent, at most that would suggest using such techniques in connection with fabricating the memory element, not the MISFETS.

At least for those reasons, the rejections of the claims should be withdrawn. A contrary conclusion would be precisely the type of improper hindsight against which the Federal Circuit has warned and would hardly be the type of "clear and particular" motivation to combine required by that Court. *See, e.g., C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998); *Teleflex, Inc. v. Ficosa North Am. Corp.*, 63 USPQ2d 1374 at 1387 (Fed. Cir. 2002).

Independent claims 1, 11 and 13 have been amended to clarify that the tunneling insulating film is formed over the gate insulating film of the MOS transistor and over the oxide film of memory cell. An example of such a structure is illustrated in FIG. 4 of the pending application in which a tunneling insulating film 16 is formed over the gate insulating film 13 of the MOS transistor and over the oxide 12 of the memory cell.

The Office action acknowledges that the Komori et al. patent does not disclose forming a tunneling insulating film, but relies on the disclosure of the Hsieh et al. patent regarding the

integrate layer 50 that separates the oxide film 45 on the floating polygate 40 from the control polygate 60 (FIG. 2f).

As already noted, however, the Hsieh et al. patent relates only to the fabrication of a memory cell, not to the fabrication of MISFETS or MOS transistors. At most, the cited references suggest forming a tunneling insulating film in connection with a memory cell. Therefore, there is no suggestion in either of the cited patents of forming a tunneling insulating film over an oxide film of a memory cell, as well as over a gate insulating film of a MOS transistor, as recited in the pending claims.

For that additional reason, applicant submits that the pending claims should be allowed.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 7/28/04

Samuel Borodach
Reg. No. 38,388

Fish & Richardson P.C.
45 Rockefeller Plaza, Suite 2800
New York, New York 10111
Telephone: (212) 765-5070
Facsimile: (212) 258-2291